CLMPTO 11/16/04

1. A method to fabricate a twin MONOS memory comprising:

forming a deep N-well in a substrate;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer;

forming an oxide mask on sidewalls of said patterned cap nitride layer;

thereafter etching through said first polysilicon layer not covered by said cap nitride layer and said oxide mask to form first trenches and removing said ONO layer exposed within said first trenches by said etching;

forming oxide spacers on sidewalls of said first trenches;

thereafter depositing a second polysilicon layer within said first trenches and recessing said second polysilicon layer below said cap nitride layer;

depositing an oxide layer overlying said recessed second polysilicon layer wherein said recessed second polysilicon layer forms raised diffusions;

etching away remaining said first polysilicon layer not covered by said oxide mask leaving control gates underlying said oxide mask wherein said ONO layer lies only underneath said control gates and leaving second trenches;

depositing a second oxide layer lining said second trenches;

thereafter depositing a third polysilicon layer within said second trenches to form word gates between each two control gates and to form word lines overlying and crossing

said word gates;

forming source and drain regions;

covering said gates with a dielectric layer; and

making contacts through said dielectric layer to said source and drain regions to form word line contacts and diffusion contacts to complete said Twin MONOS memory device.

2. The method according to Claim 1 wherein said step of forming said oxide-nitride-oxide (ONO) layer comprises:

thermally growing a base oxide layer on said substrate surface;

nitridizing said base oxide layer in a NH_3 ambient;

depositing a nitride layer overlying said nitridized base oxide layer;

depositing a top oxide layer overlying said nitride layer; and

oxidizing said nitride layer to stabilize a boundary between about nitride layer and said top oxide layer .

3. The method according to Claim 2 further comprising annealing said nitride layer in NO after depositing said nitride layer.

4. The method according to Claim 2 further comprising annealing said ONO layer in NH_3 or N_2O.

5. The method according to Claim 1 wherein said step of forming said oxide-nitride-

oxide (ONO) layer comprises:

thermally growing a base oxide layer on said substrate surface;

nitridizing said base oxide layer in a NH_3 ambient;

depositing a nitride layer overlying said base oxide layer; and

oxidizing said nitride layer to form a top oxide layer overlying said nitride layer.

6. The method according to Claim 5 wherein said nitride layer is a silicon-rich nitride layer.

7. The method according to Claim 5 further comprising annealing said ONO layer in NH_3 or N_2O.

8. The method according to Claim 1 further comprising annealing said twin MONOS memory in H_2 after contact open process

9. The method according to Claim 1 wherein when electrons stored in a nitride portion of said ONO layer are to be erased through a bottom oxide portion of said ONO layer, a bottom oxide portion is thinner than a top oxide portion of said ONO layer.

10. The method according to Claim 1 wherein when electrons stored in a nitride portion of said ONO layer are to be erased through a top oxide portion of said ONO layer, a top oxide portion is thinner than a bottom oxide portion of said ONO layer.

11. The method according to Claim 1 wherein said oxide mask has a thickness of between about 20 and 80 nm.

12. The method according to Claim 1 further comprising implanting p-type dopant into said first polysilicon layer to eliminate an electron source through said ONO layer during F-N erase operation.

13. The method according to Claim 1 further comprising implanting boron or BF_2 ions at a tilt angle into said substrate under said first polysilicon layer to form a control gate channel.

14. The method according to Claim 13 further comprising implanting lightly doped n-type dopant into said control gate channel to prevent hole accumulation during F-N erase operation.

15. The method according to Claim 1 after said step of removing said ONO layer exposed within said trenches, further comprising implanting ions to form LDD regions.

16. The method according to Claim 1 wherein said raised diffusions form bit diffusions between said control gates to reduce bit resistance.

17. The method according to Claim 1 wherein said second polysilicon layer is recessed 50 to 150 nm from a top surface of said cap nitride layer.

18. The method according to Claim 1 wherein said word gate is a step word gate wherein said substrate is etched into a short distance during said step of forming said second trenches.

19. The method according to Claim 1 wherein said second trenches have a positive slope.

20. The method according to Claim 1 further comprising saliciding word lines.

21. A method to fabricate a twin MONOS memory in a CMOS process comprising:

providing a memory area and a CMOS area separated by isolation regions in a substrate;

forming a deep N-well in said memory area;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer in said memory area;

forming an oxide mask on sidewalls of said patterned cap nitride layer in said memory area;

thereafter etching through said first polysilicon layer not covered by said cap nitride and said oxide mask to form trenches and removing said ONO layer exposed within said trenches by said etching in said memory area;

forming oxide spacers on sidewalls of said trenches;

thereafter depositing a second polysilicon layer within said trenches and recessing said second polysilicon layer below said cap nitride layer;

depositing an oxide layer overlying said recessed second polysilicon layer wherein said recessed second polysilicon layer forms raised diffusions;

etching away remaining said first polysilicon layer not covered by said oxide mask leaving control gates underlying said oxide mask wherein said ONO layer lies only underneath said control gates and leaving second trenches;

patterning said first polysilicon layer in said CMOS area to form logic gates;

depositing a second oxide layer lining said second trenches and covering said logic gates;

thereafter depositing a third polysilicon layer in said memory area within said second trenches to form word gates between each two control gates and to form word lines overlying and crossing said word gates;

forming source and drain regions in said CMOS area and in said memory area;

covering said logic gates and said gates in said memory area with a dielectric layer; and

making contacts through said dielectric layer to said source and drain regions to form word line contacts and diffusion contacts to complete said Twin MONOS memory device.

22. The method according to Claim 21 wherein said step of forming said oxide-nitride-oxide (ONO) layer comprises:

thermally growing a base oxide layer on said substrate surface;

nitridizing said base oxide layer in a NH_3 ambient;

depositing a nitride layer overlying said nitridized base oxide layer;

depositing a top oxide layer overlying said nitride layer; and

oxidizing said nitride layer to stabilize a boundary between about nitride layer and said top oxide layer .

23. The method according to Claim 21 wherein said step of forming said oxide-nitride-oxide (ONO) layer comprises:

thermally growing a base oxide layer on said substrate surface;

nitridizing said base oxide layer in a NH_3 ambient;

depositing a nitride layer overlying said base oxide layer; and

oxidizing said nitride layer to form a top oxide layer overlying said nitride layer.

24. The method according to Claim 21 wherein when electrons stored in a nitride portion of said ONO layer are to be erased through a bottom oxide portion of said ONO layer, said bottom said oxide portion is thinner than a top oxide portion of said ONO layer.

25. The method according to Claim 21 wherein when electrons stored in a nitride portion of said ONO layer are to be erased through a top oxide portion of said ONO layer, a top oxide portion is thinner than a bottom oxide portion of said ONO layer.

26. The method according to Claim 21 wherein said oxide mask has a thickness of between about 20 and 80 nm.

27. The method according to Claim 21 further comprising implanting p-type dopant into said first polysilicon layer to eliminate an electron source through said ONO layer during F-N erase operation.

28. The method according to Claim 21 further comprising implanting boron or BF_2 ions at a tilt angle into said substrate under said first polysilicon layer to form a control gate channel.

29. The method according to Claim 21 further comprising implanting lightly doped n-type dopant into said control gate channel to prevent hole accumulation during F-N erase operation.

30. The method according to Claim 21 wherein said second polysilicon layer is recessed 50 to 150nm from a top surface of said cap nitride layer.

31. The method according to Claim 21 wherein said word gate is a step word gate wherein said substrate is etched into a short distance during said step of forming said second trenches.

32. The method according to Claim 21 after said step of removing said ONO layer exposed within said first trenches, further comprising implanting ions to form LDD regions.

33. The method according to Claim 21 further comprising saliciding said word lines.

34. A method to fabricate a twin MONOS memory in a CMOS process comprising:

providing a memory area and a CMOS area separated by isolation regions in a substrate;

forming a deep N-well in said memory area;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer in said memory area;

forming an oxide mask on sidewalls of said patterned cap nitride layer in said memory area;

thereafter etching through said first polysilicon layer not covered by said cap nitride and said oxide mask to form trenches and removing said ONO layer exposed within said trenches by said etching in said memory area;

forming oxide spacers on sidewalls of said trenches;

thereafter depositing a second polysilicon layer within said trenches and recessing said second polysilicon layer below said cap nitride layer;

depositing an oxide layer overlying said recessed second polysilicon layer wherein said recessed second polysilicon layer forms raised diffusions;

etching away remaining said first polysilicon layer not covered by said oxide mask leaving control gates underlying said oxide mask wherein said ONO layer lies only underneath said control gates and leaving second trenches;

depositing a second oxide layer lining said second trenches;

thereafter depositing a third polysilicon layer in said memory area within said second trenches to form word gates between each two control gates and to form word lines overlying and crossing said word gates and patterning said third polysilicon layer in said CMOS area to form logic gates;

forming source and drain regions in said CMOS area and in said memory area;

covering said logic gates and said gates in said memory area with a dielectric layer; and

making contacts through said dielectric layer to said source and drain regions to form word line contacts and diffusion contacts to complete said Twin MONOS memory device.

CLAIMS 35-47 (CANCELLED)

48. A method to fabricate a twin MONOS memory comprising:

forming a deep N-well in a substrate;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer;

CLAIMS 49-50 (CANCELLED)

51. A method to fabricate a twin MONOS memory comprising:

forming a deep N-well in a substrate;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer;

forming an oxide mask on sidewalls of said patterned cap nitride layer;

etching away said cap nitride leaving a looped said oxide mask on said first polysilicon layer;

selectively cutting said looped oxide mask at both ends of a block into two lines wherein adjacent control lines of adjacent loops are cut alternately;

thereafter etching away said first polysilicon layer not covered by said oxide mask and said underlying ONO layer, leaving control gates underlying said oxide mask wherein said ONO layer lies only underneath said control gates and leaving trenches;

implanting source/drain diffusions into said substrate underlying said trenches;

thereafter filling said trenches with oxide;

thereafter forming a common source line and bit contacts to some of said source/drain diffusions; and

forming bit line contacts and control gate contacts and connecting said bit contacts along said bit line by an overlying metal line to complete said Twin MONOS memory device.

CLAIMS 52-56 (CANCELLED)

57. A method to fabricate a twin MONOS memory comprising:

forming a deep N-well in a substrate;

forming an oxide-nitride-oxide (ONO) layer overlying said substrate;

depositing a first polysilicon layer overlying said ONO layer;

depositing a cap nitride layer overlying said first polysilicon layer;

patterning said cap nitride layer to said first polysilicon layer;

forming an oxide mask on sidewalls of said patterned cap nitride layer;

etching away said cap nitride leaving a looped said oxide mask on said first polysilicon layer;

selectively cutting said looped oxide mask at both ends of a block into two lines wherein adjacent control lines of adjacent loops are cut alternately;

thereafter etching away said first polysilicon layer not covered by said oxide mask and said underlying ONO layer, leaving control gates underlying said oxide mask wherein said ONO layer lies only underneath said control gates and leaving trenches;

implanting source/drain diffusions into said substrate underlying said trenches;

thereafter filling said trenches with oxide;

thereafter forming local contacts to said source diffusions to form common source lines;

forming bit contacts to said drain diffusions and connecting said bit contacts along said bit line by an overlying metal line; and

forming control gate contacts to complete said Twin MONOS memory device.

CLAIMS 48-62 (CANCELLED)